WHAT IS CLAIMED IS:

1. An integrator circuit comprising:

(a) an input conductor for conducting an input current;

(b) an amplifier stage having an input coupled to the input conductor;

(c) an integrating capacitor coupled between the input of the amplifier stage and an output of the amplifier stage; and

(e) an MOS capacitor coupled between an output of the amplifier stage and a voltage conductor for biasing the MOS capacitor.

2. An integrator circuit comprising:

(a) an input conductor for conducting an input current;

(b) a first amplifier stage having an input coupled to the input conductor ;

(c) a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage;

(d) an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage; and

(e) an MOS compensation capacitor coupled between the input and output of the second amplifier stage.

3. The integrator circuit of claim 2 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

4. The integrator circuit of claim 3 wherein the first and second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region

for high values of the input current to provide a low value of compensation capacitance for the integrator circuit.

5. The integrator circuit of claim 4 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a higher amount of noise for the high values of the input current, and wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

6. The integrator circuit of claim 2 wherein the first amplifier stage is a non-inverting amplifier stage and the second amplifier stage is an inverting amplifier stage.

7. The integrator circuit of claim 2 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of

the second amplifier stage.

8. The integrator circuit of claim 7 wherein the integrating capacitor is a poly capacitor.

9. The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a single-ended input signal.

10. The integrator circuit of claim 2 wherein the input of the first amplifier stage conducts a differential input signal.

11. The integrator circuit of claim 6 wherein the second stage amplifier is an inverting class A amplifier.

12. A CT scanner data acquisition system comprising:

(a) a plurality of integrator circuits, each including

i. an input conductor for conducting an input current,

ii. a first amplifier stage having an input coupled to the input conductor,

iii. a second amplifier stage having an output and also having an input coupled to an output of the first amplifier stage,

iv. an integrating capacitor coupled between the input of the first amplifier stage and the output of the second amplifier stage, and

v. an MOS compensation capacitor coupled between the input and output of the second amplifier stage;

(b) a plurality of photodiodes each having an anode coupled to an input conductor of an integrator circuit, respectively;

(c) a plurality of analog-to-digital converters, inputs of the analog-to-digital

converters being coupled to the outputs of various integrator circuits.

13. The CT scanner data acquisition system of claim 12 wherein the first amplifier stage includes an input stage having an output coupled to an input of a folded cascode stage, an output of the folded cascode stage being coupled to a first terminal of the MOS capacitor, a second terminal of the MOS capacitor being coupled to the output of the second amplifier stage.

14. The CT scanner data acquisition system of claim 13 wherein the second amplifier stages co-act to establish bias voltage across the MOS capacitor so as to bias the MOS capacitor in its accumulation region for low values of the input current to provide a high value of compensation capacitance for the integrator circuit and so as to bias the MOS capacitor in its inversion region for high values of the input current to provide a low value of compensation capacitance for the integrator circuit.

15. The integrator circuit of claim 14 wherein the input current is a photodiode current containing a relatively low amount of noise for the low values of the input current and containing a relatively high amount of noise for the high values of the input current, wherein an amount of noise produced by the integrator circuit when the value of the compensation capacitance is high is masked by the relatively high amount of noise.

16. The CT scanner data acquisition system of claim 12 wherein the analog-to-digital converters are delta-sigma analog-to-digital converters.

17. The CT scanner data acquisition system of claim 12 wherein the inputs of the analog-to-digital converters are coupled to common outputs of groups of the integrator circuits, respectively.

18. The CT scanner data acquisition system of claim 12 wherein the first amplifier stage is an operational amplifier stage and the second amplifier stage is an inverting amplifier stage.

19. The CT scanner data acquisition system of claim 12 wherein the MOS compensation capacitor includes an N-channel source region and an N-channel drain region both coupled to the input of the second stage amplifier, and also includes a gate disposed over a channel region between the N-channel source region and the N-channel drain region, the gate being coupled to the output of the second amplifier stage.

20. The CT scanner data acquisition system of claim of 19 wherein the integrating capacitor is a poly capacitor.

21. The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a single-ended input signal.

22. The CT scanner data acquisition system of claim 12 wherein the input of the first amplifier stage conducts a differential input signal.

23. The CT scanner data acquisition system of claim 12 wherein the second stage amplifier is an inverting class A amplifier.

24. A method of operating an integrator circuit comprising:

(a) conducting an input current into an input of an amplifier stage;

(b) charging an integrating capacitor coupled between the input and an output of the amplifier stage in response to the input current; and

(c) compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS capacitor coupled to the output into a predetermined operating region range.

25. A method of operating an integrator circuit, comprising:

(a) conducting an input current into an input conductor of a first amplifier

stage;

(b) coupling an input of a second amplifier stage to an output of the first amplifier stage;

(c) charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

(e) compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range.

26. A method of operating a CT scanner data acquisition system, comprising:

(a) in each of a plurality of integrator circuits,

i. conducting an input current into an input conductor of a first amplifier stage,

ii. coupling an input of a second amplifier stage to an output of the

first amplifier stage,

iii. charging an integrating capacitor coupled between the input of the first amplifier stage and an output of the second amplifier stage; and

iv. compensating the integrator circuit by controlling the bandwidth of the integrator circuit by biasing an MOS compensation capacitor coupled between the input and output of the second amplifier stage into a predetermined operating region range;

(b) coupling an anode of each of a plurality of photodiodes to an input conductor of a group of integrator circuits, respectively;

(c) coupling inputs of a plurality of analog-to-digital converters to the outputs of various groups of integrator circuits, respectively.